REMARKS

Reconsideration of the application is requested.

Applicants acknowledge the Examiner's confirmation of receipt of Applicants' certified copy of the priority document for German Patent Application 100 17 362.4, filed April 7, 2000 supporting the claim for priority under 35 U.S.C. § 119.

Claims 1-11 remain in the application. No claims have been amended, added or canceled.

In "Claim Rejections - 35 USC § 103" on pages 2-5 of the above-identified Office Action, claims 1-5 and 7-11 have been rejected as being obvious over U.S. Patent No. 5,845,130 to Goff et al. (hereinafter Goff), under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the reference.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claims 1, 9, 10 and 11 each call for, *inter alia*:

an input control information memory ... storing an item

of binary control information for each of the memory

blocks of the input memory; and

an output control information memory ... storing an item

of binary control information for each of the memory

blocks of the output memory.

The Goff reference discloses a mailbox traffic controller

system having two processors 200, 208 coupled to a shared

memory 202. The shared memory 202 includes an array of

read/write registers (column 3, lines 46, 47 of Goff).

Further, the system includes a traffic controller 204 which

controls access of the processors 200, 208 to the shared

memory 202. To that end, a processor 200, 208 which intends

to access the shared memory 202 writes its identifier into

the traffic controller 204. The processor 200, 208 gains

access to the entire shared memory 202 by writing its

identifier into the traffic controller 204. If a processor

200, 208 desires to control access to the shared memory 202

and, when reading the traffic controller 204, finds the

identifier of the other processor 208, 200 already stored

therein, the requesting processor 202, 208 knows that it must

wait before attempting to control access to the shared memory

202 (column 4, lines 27 to 32 of Goff).

As stated above, claim 1 of the instant application calls for
"an input control information memory ... storing an item of
binary control information for each of said memory blocks of
said input memory" and "an output control information memory
... storing an item of binary control information for each of
said memory blocks of said output memory." Claims 9, 10 and
11 contain similar limitations.

Therefore, the subject matter of claims 1, 9, 10 and 11 of
the instant application is distinguished in two respects from
the circuit disclosed in Goff:

> - The traffic controller 204 fails to handle control
> information which refers to the individual registers of
> the shared memory 202 (which correspond to the
> individual memory blocks of the input or output memory
> as recited in claims 1, 9, 10 and 11 of the instant
> application). Thus, the traffic controller 204 is not
> in a position to monitor or control blockwise access to
> the shared memory 202. Quite the contrary, the
> identifier recorded in the traffic controller 204
> constitutes control information relating to the entire
> shared memory 202.

- The traffic controller 204 fails to operate on binary

control information. As explained in column 4, lines 4

to 6 and lines 19 to 24 of Goff, the traffic controller

204 stores a zero (indicating that no processor

currently controls access to shared memory 202), an

identifier of the first processor 200 (identifying that

processor 200 currently controls access to the shared

memory 202) or an identifier of the second processor 208

(identifying that processor 208 currently controls

access to the shared memory 202). Thus, since at least

three different values must be storable in the traffic

controller 204 for controlling memory access, Goff fails

to teach using an item of binary control information for

memory access control.

As a result, the subject matter of claims 1, 9, 10 and 11 of

the instant application is not disclosed by Goff.

Moreover, the subject matter of claims 1, 9, 10 and 11 is

non-obvious over the teaching of Goff.

It is noted that not only is the structure recited in the

claims of the instant application different from that of

Goff, but the purpose of the traffic controller 204 is also

different from the purpose of the input or output control

information memories recited in the claims of the instant

application. More specifically, the traffic controller 204

ensures that only one of the processors 200, 208 obtains

access control to the (entire) shared memory 202. That

prevents access contention, however, it does not prevent data

written from one of the processors 200, 208 from being

overwritten later before being read. In contrast thereto,

the provision of blockwise binary control information

according to the present invention makes it possible to block

rewriting before read-out of a memory block. Therefore,

since two different memory control approaches (control for

preventing access contention versus control for preventing

data overwriting before read-out) are used in Goff and the

present invention as claimed, there is neither a motivation

nor a straightforward way to apply the teaching of Goff for

meeting the object underlying the present invention.

Clearly, Goff does not show an input control information

memory storing an item of binary control information for each

of the memory blocks of the input memory, nor an output

control information memory storing an item of binary control

information for each of the memory blocks of the output

memory, as recited in claims 1, 9, 10 and 11 of the instant

application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1, 9, 10 and 11. Claims 1, 9, 10 and 11 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

Finally, applicants appreciatively acknowledge the Examiner's statement that claim 6 is merely objected to as being dependent upon a rejected base claim. In light of the above, Applicants respectfully believe that rewriting of claim 6 is unnecessary at this time.

In view of the foregoing, reconsideration and allowance of claims 1-11 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.
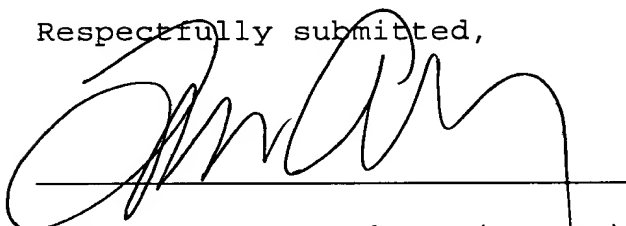
If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith

should be charged to the Deposit Account of Lerner and

Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect

to Sections 1.16 and 1.17 to the Deposit Account of Lerner

and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

Laurence A. Greenberg (29,308)

LAG/bb

March 7, 2005

Lerner and Greenberg, P.A.
P.O. Box 2480
Hollywood, Florida 33022-2480
Tel.: (954) 925-1100
Fax: (954) 925-1101